increases in proportion to the square of the input differential voltage. It is also possible to drive the differential pair by a constant current source. A level shifter may be provided for level-shifting the addition output voltage from the commonly coupled source electrodes.

**IN THE CLAIMS:**

**The claims are amended as follows:**

1. A voltage subtractor/adder circuit comprising:

a differential pair having first and second MOS transistors, gate electrodes of said first and second MOS transistors forming input terminals for receiving an input differential voltage, drain electrodes of said first and second MOS transistors forming output terminals for outputting a signal to be subtracted, and source electrodes of said first and second MOS transistors being commonly coupled to form an output terminal outputting a voltage to be added; and

wherein the sum of currents flowing through said first and second MOS transistors increases in proportion to the square of said input differential voltage.

3. A voltage subtractor/adder circuit comprising:

a differential pair having first and second MOS transistors, gate electrodes of said first and second MOS transistors forming input terminals for receiving an input differential voltage, drain electrodes of said first and second MOS transistors forming output terminals for outputting a signal to be subtracted, and source electrodes of said first and second MOS transistors being commonly coupled to form an output terminal for outputting a voltage to be added; and

a constant current source which drives said differential pair.